Mips Adds a New Dimension to MIPS64

Yet another company is retrofitting a CPU architecture with new instructions for 3D graphics—this time, even before the first chip based on the architecture comes out. Mips Technologies has introduced MIPS-3D, a set of 13 instructions for MIPS64 embedded processors.

MIPS64 is a 64-bit architecture announced earlier this year at Embedded Processor Forum, along with MIPS32 (see MPR 5/31/99, p. 18). It's based on the MIPS-V instruction set, which already has some single-instruction multiple-data (SIMD) operations for floating-point math. Those instructions can operate on pairs of single-precision numbers in 64-bit registers. Single-precision numbers are commonly used for geometry calculations in 3D graphics.

As Table 1 shows, MIPS-3D takes advantage of the existing "paired-single" instructions by adding new instructions for matrix multiplication, image clipping, lighting, and other tasks. There are no new registers; MIPS-3D employs the 32 floating-point registers already defined in MIPS64.

According to Mips's estimates, MIPS-3D will speed 3D graphics by as much as 83% over the older MIPS-IV architecture. At 500 MHz, a MIPS-3D chip can transform the vertex of a polygon and apply lighting effects in 49 cycles, compared with 90 cycles for a MIPS-IV chip running at the same clock frequency. That should allow the processor to draw 10 million polygons per second with lighting, or 25 million polygons without lighting.

Those are estimates, however, because there aren't any MIPS64 chips available yet. Mips has licensed its first chip design with MIPS-3D, the R20K, to NEC and Toshiba, but it isn't expecting first silicon until the first half of next year. A hard-core version, the 20Kc "Ruby," is expected from Mips next year, too. Mips will reveal details about a MIPS64 soft core at Microprocessor Forum in October, but that core—known as the 5Kc "Opal"—won't use MIPS-3D.

Because it adds only 13 instructions and no new registers, MIPS-3D won't occupy much silicon. Mips says the extension will add less than 0.5 mm^2 of die area to a chip manufactured in a 0.25-micron IC process.

Name	Description	Latency
ADDR	FP add (store 32b results in 64b register)	5 cycles
MULR	FP multiply (store 32b results in 64b reg)	5 cycles
RECIP1	Reciprocal with reduced-precision result	5 cycles
RECIP2	Reciprocal, 2nd step	4 cycles
RSQRT1	Reciprocal square root with reduced result	5 cycles
RSQRT2	Reciprocal square root, 2nd step	4 cycles
CVT.PS.PW	Convert two 32b ints to FP paired single	4 cycles
CVT.PW.PS	Convert FP paired single to two 32b ints	4 cycles
CABS	FP absolute compare	4 cycles
BC1ANY2F	Branch if any 2 conditions false	1 cycle
BC1ANY2T	Branch if any 2 conditions true	1 cycle
BC1ANY4F	Branch if any 4 conditions false	1 cycle
BC1ANY4T	Branch if any 4 conditions true	1 cycle

Table 1. All MIPS-3D instructions except branches have single-cycle throughput; branches c an repeat every two cycles.

Even with MIPS-3D, a 500-MHz MIPS64 processor won't deliver anything close to the 3D-graphics performance of the 300-MHz Emotion Engine (see MPR 4/19/99, p. 1) that Sony and Toshiba designed for the next-generation PlayStation. Sony and Toshiba created their own extensions for that MIPS-compatible chip. But MIPS-3D isn't shooting for the high-end video-game market; it's for digital set-top boxes, information appliances, handheld computers, lower-end game machines, and other products that need good but not groundbreaking graphics performance.

MIPS-3D is more focused on 3D graphics than recent extensions from SandCraft (see MPR 7/12/99, p. 10) and Lexra (see MPR 8/23/99, p. 19). The MIPS64 architecture already includes some instructions for digital signal processing. The main advantage of MIPS-3D is that it's blessed by the Mips mothership, so some licensees may feel more comfortable adopting it. —*T.R.H.*

Arm Announces Two Soft Cores With DSP

Arm has unveiled two synthesizable cores based on the ARM9E announced at Embedded Processor Forum last spring (see MPR 6/21/99, p. 11). Both include the ARM9E's digital-signal processing (DSP) extensions and the high-speed AMBA (Advanced Microcontroller Bus Architecture) on-chip interface. They are binary-compatible with the ARM7, ARM9, ARM10, and StrongArm families.

The ARM966E-S is a cacheless core that relies on tightly coupled on-chip SRAM for fast access to instructions and data. It's intended for hard real-time applications—such as hard-disk servos and automotive-control systems—that might be disrupted by the unpredictability of caches.

The '966E-S can address up to 64M of tightly coupled SRAM and can address the full 4G address space on the AMBA bus. These address spaces pose no real limit, because embedded applications rarely need that much memory. Excluding memory, the '966E-S has 90,000–100,000 gates.

In contrast, the ARM946E-S is a more conventional design with four-way set-associative caches. Some of Arm's hard cores with custom layouts have 64-way caches, but four-way associativity allows ASIC designers to use standard SRAM blocks in macrocell libraries. Excluding caches, the '946E-S has about 150,000 gates.

Arm expects chips based on these cores to run at about 160 MHz in a 0.25-micron IC process and at least 200 MHz in 0.18 micron. At 200 MHz, the estimated performance is 220 Dhrystone 2.1 MIPS. Arm says the chips will consume only slightly more power than those based on ARM9-series hard cores. Arm plans to deliver the RTL code for both cores in 1Q00, and LSI is one of the first licensees. —*T.R.H.* M