First StarCore DSP Targets Networking

Motorola's MSC8101 Combines SC140 Core and PowerQuicc II Coprocessor

by Tom Halfhill

Motorola's latest digital-signal processor is so network oriented that the company has considered inventing a new buzzword for it: NetDSP.

The new MSC8101 is the first DSP to emerge from the StarCore alliance between Motorola and Lucent. Although it's based on the SC140 core that the companies jointly developed (see MPR 5/10/99, p. 13), it's a Motorola product that draws heavily on Motorola's expertise in communications processing. It's designed for networking and telephony applications—particularly those that need real-time digital filtering, such as speech compression and echo cancellation.

Most of the heavy lifting will be done by the SC140 core, a six-issue VLIW DSP with 16 function units, including four multiply-accumulate (MAC) units that can execute 1.2 billion MACs/s at the chip's target frequency of 300 MHz. As Figure 1 shows, this core also has 512K of tightly coupled SRAM for storing instructions and data plus a 16-bit host interface for external microcontrollers.

To assist the SC140, Motorola added a coprocessor module extracted from its MPC8260 PowerQuicc II processor (see MPR 9/14/98, p. 12). The coprocessor, which Motorola also calls a "programmable protocol engine," runs at 150 MHz. It executes protocol-specific microcode stored in on-chip ROM, which can be overridden by 24K of on-chip RAM. It has some serial I/O interfaces, timers, and other integrated peripherals, and it supports network connections to 155-Mbps ATM, 10/100-Mbps Ethernet, up to four 1.5-Mbps T1/E1 lines, or one 45-Mbps T3/E3 line plus one T1/E1 line.

In a network router, the primary job of this coprocessor is to perform layer-2 and layer-3 analysis on packet headers to determine whether the DSP section needs to handle the packets or not. For instance, if the coprocessor analyzes a header and discovers that the packet contains voice-over-IP (VoIP) data, it can divert the packet to the SC140's internal buffer for digital filtering. The coprocessor can also perform segment-and-reassembly (SAR) operations on ATM cells. This reduces the overhead on the SC140 core, which receives an interrupt only when a whole packet or frame arrives in its internal buffer.

Another module, known as the enhanced filter coprocessor (EFCOP), is appended to the SC140 core. It runs at 300 MHz and is optimized for tasks such as echo cancellation. A centralized 16-channel DMA engine helps to keep the processor fed with data.

Note that the MSC8101 is not primarily designed for packet switching in high-end routers. That task would still be performed by the router's general-purpose CPU and ASICs, or by specialized network processors such as those recently announced by Intel (see MPR 9/13/99, p. 1), C-Port, and IBM Microelectronics (see MPR 10/6/99, p. 18).

The MSC8101 inherits more from the PowerQuicc II than a coprocessor module. Unique among DSPs, it also has a PowerPC 60x-compatible system bus. The 100-MHz bus works with 32- and 64-bit peripherals and can connect to other PowerPC processors in master/slave or multimaster configurations. The peak bandwidth is 800 MBytes/s. This bus allows designers to build routers and other systems with multiple MSC8101 DSPs and PowerPC processors in complex switching fabrics. The DSPs in a multichip configuration can access the internal memory of the others over the PowerPC bus.

Motorola plans to sample the MSC8101 to favored customers in 2Q00, with general sampling following soon afterward. The company hasn't announced when production will begin, but the price is expected to be $98 in 10,000-unit quantities. Power consumption is low for such a highly integrated 300-MHz device: about 500 mW at 1.5 V. That's in Motorola's 0.18-micron copper HiPerMOS-6 process.

We're still waiting for the other chip to drop—Lucent's first StarCore DSP. Under terms of their partnership, Motorola and Lucent collaborate on StarCore architectures, cores, and basic development tools, but each partner designs its own chips. Motorola appears to have beaten Lucent to the punch by adapting some proven technology from its PowerPC and PowerQuicc II lines to create a powerful DSP for communications and networking applications. M

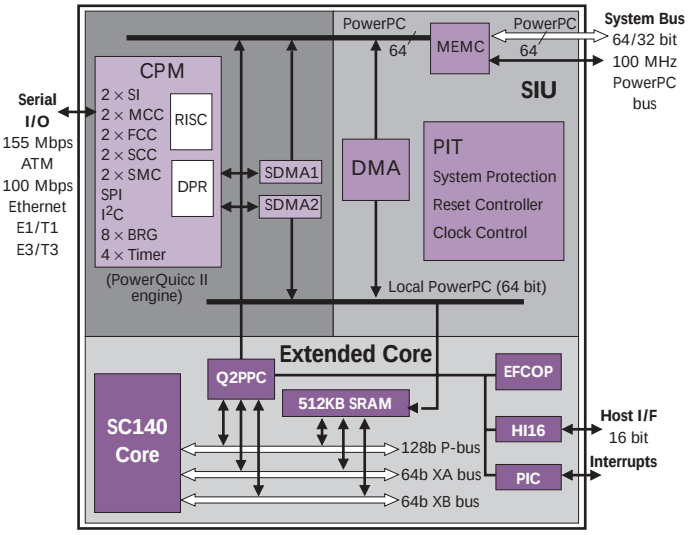

Figure 1. Motorola's MSC8101 DSP combines a StarCore SC140 core with a PowerQuicc II protocol-processing engine.