IBM, C-Port Network Processors Challenge Intel

At about the same time as Intel's IXP1200 announcement (see MPR 9/13/99, p. 1), C-Port and IBM Microelectronics separately announced two network processors aimed at the same market—high-speed routers and related communications equipment. C-Port and IBM have also created an industry forum to develop common APIs that will run on network processors from different companies. The sudden flurry of news underscored the importance of this fast-growing processor category.

All three companies plan to begin volume production in 2000, but IBM's processor will come later than the others. Although these chips vary widely in terms of architecture, integration, and price, they're promising the same things: higher performance than discrete RISC processors in specific networking applications, the programmability that's lacking in fixed-function ASICs, and shorter development cycles for router vendors that are trying to keep up with burgeoning network traffic.

The C-5's additional claim to fame is that it's easy to program in C or C++ instead of assembly language, according to C-Port. The company says it spent half of its development costs on creating software tools. In contrast, Intel's development suite for the IXP1200 is based on a symbolic assembler—a very good symbolic assembler, by all appearances, but an assembler nonetheless.

Of course, the RISC processors in today's routers have always been programmable in high-level languages. But network processors have new architectures and instruction sets that are optimized for packet routing, address-table management, and other specialized networking tasks. It remains to be seen how effective high-level languages and compilers will be at those tasks.

The new CPIX (Common Programming Interfaces) Forum created by C-Port and IBM is also intended to assist developers. CPIX's goal is to specify APIs that will make it easier to port code from one network processor to another, even if the architectures are completely different. CPIX is associated with the CSIX (Common Switch Interfaces) Consortium *(www.csix.org)*, which is developing similar specifications for high-speed switch fabrics. At this writing, Intel has not expressed an interest in joining CPIX.

Developers would welcome anything that makes network processors easier to program, because these chips all have unusually complex microarchitectures. C-Port's C-5 integrates 16 channel processors that receive, process, and transmit cells and packets, plus five on-chip coprocessors that offload table lookups, memory management, and other router-specific tasks. IBM's Network Processor integrates a PowerPC 40x core with 10 picoprocessors (RISC cores) that handle such things as packet processing, table lookups, and data queuing. Intel's IXP1200 integrates a StrongArm core and six microengines (RISC cores) on a single chip.

C-Port is sampling the 200-MHz C-5 now; volume production is scheduled to begin in 1Q00, with quantity pricing starting at $400. IBM will begin sampling its 133-MHz Network Processor in 4Q99. Samples are built in a 0.25-micron IC process, but IBM will port the design to a 0.18-micron copper process before mass production begins in mid-2000. IBM has not disclosed pricing. Intel's 166-MHz IXP1200 is sampling in limited quantities now; general sampling begins in 4Q99, and volume production is scheduled for 1Q00. Intel hasn't announced volume pricing, but the sample price is only $200.

In the absence of production silicon and reliable benchmarks, it's almost impossible to compare the performance of these devices. For layer-3 routing, C-Port says the C-5 can handle two OC-48 lines at wire speed; that's 5 Gbps or about 16.7 million 40-byte TCP packets per second. IBM says its Network Processor can handle four Gigabit Ethernet links; that's 4 Gbps or about 8.3 million packets per second—but the minimum size for Ethernet packets is 64 bytes, not 40 bytes. Intel says the primary bus interface on the IXP1200 has about 4.1 Gbps of bandwidth and that the chip can perform layer-3 routing for 2.5 million 64-byte packets per second.

Keep in mind that all of these processors are designed to work with even more specialized companion chips and external coprocessors, so the design of the router will have a much greater impact on real-world performance than the somewhat abstract numbers quoted by the semiconductor vendors. The key differentiating factors are likely to be cost, ease of programmability, the capabilities of their companion chips, and sustainable bandwidth when a router uses multiple processors in a complex switching fabric. —*T.R.H.*

Triscend Ships First Reconfigurable 8051

When nothing but a malleable microcontroller will do, Triscend has the solution: a chip that combines an 8051-compatible processor core with reconfigurable logic. The first member of Triscend's E5 family—called the TE520—is now in full production, with additional members to follow next year. Triscend (see MPR 11/16/98, p. 12) is also developing a version based on a much more powerful 32-bit ARM7TDMI core.

In the meantime, the 40-MHz TE520 isn't exactly a speed demon at 10 MIPS, but start-up Triscend hopes it will fill a niche. The chip has 2,048 configurable-logic cells (enough for about 25,600 gates) and 40K of on-chip RAM. It's intended for quick-to-market embedded applications that need a custom system on a chip but that probably won't reach high enough production volumes to justify the expense of developing an ASIC. Customers can configure the TE520's logic to create on-chip peripherals specific to their applica-

tions—and even to reconfigure the logic in the field if the applications change.

Triscend says it already has customers for the TE520, although they prefer not to be named. One customer is using the TE520 in a PC Card wireless receiver that picks up signals from tiny beacons attached to shipping containers; it allows workers in the field to keep track of shipping logistics. Another customer is using the TE520 to replace a discrete 8051 microcontroller and programmable-logic chips in the channel concentrator of a telephone line card; the TE520 takes up less room, allowing more of the devices to fit into tight spaces.

The TE520 isn't the most economical way to build an 8051-based system if configurability isn't important. It costs $45 in 100-unit quantities and $25 in 100,000-unit quantities, while discrete 8051 chips are commonly available for less than the price of a movie ticket. But the universe of embedded applications is large, and some of those applications undoubtedly can take advantage of the TE520's unique features. Triscend says future members of the E5 family will have amounts of configurable logic varying from 512 to 3,200 cells (about 6,400 to 40,000 gates), 16K to 64K of on-chip RAM, and volume prices as low as $8 next year. The ARM-based version is scheduled to debut in 1H00. —*T.R.H.*

MIPS32 4Km Core Has Fast MAC

Mips Technologies' new 4Km is the third synthesizable core to adopt the MIPS32 instruction-set architecture introduced earlier this year for embedded applications. The 4Km combines features of the MIPS32 4Kc and 4Kp cores, which were disclosed at Embedded Processor Forum in May (see MPR 5/31/99, p. 18).

As the table below shows, the 4Km is almost identical to the 4Kc and 4Kp, except for two features: memory management and math. The 4Km manages memory by using block-address translation (BAT), and it has a fast integer multiply-divide unit. In contrast, the 4Kc has a memory-management unit (MMU) with a 32-entry translation-lookaside buffer (TLB) instead of a BAT, while the 4Kp has a slower, iterative multiply-divide unit instead of the fast multiplier.

In terms of capability, then, the new core is halfway between the other two cores. It's good at math, but it doesn't have an MMU. One consequence is that it can't run Windows CE, which requires an MMU.

The fast multiplier can execute a 32 × 16 → 64-bit multiply-accumulate (MAC) instruction in a single cycle, or a 32 × 32 → 64-bit MAC in two cycles. That's identical to the performance of the 4Kc but much faster than the 4Kp, which needs 34 cycles to execute a 32 × 16 → 64-bit MAC. The tradeoff, as seen in the table, is a slightly larger die, but the difference is negligible. (In the table, the die-size and power-consumption figures exclude caches. All of those numbers are estimates, due to variations in IC processes.)

Core Feature	4Km	4Kc	4Kp
MIPS ISA	MIPS32	MIPS32	MIPS32
Freq (0.18µ)	200–280 MHz	200–280 MHz	200–280 MHz
Freq (0.25µ)	150–200 MHz	150–200 MHz	150–200 MHz
Perf (0.18µ)*	240–335 MIPS	240–335 MIPS	240–335 MIPS
Perf (0.25µ)*	180–240 MIPS	180–240 MIPS	180–240 MIPS
L1 Cache Sizes	0–16KB	0–16KB	0–16KB
Fast Multiplier?	Yes	Yes	No
Memory Mgmt	BAT	MMU	BAT
Windows CE?	No	Yes	No
Die Size (0.18µ)	1.4 mm^2	1.5 mm^2	1 mm^2
Die Size (0.25µ)	2.8 mm^2	3 mm^2	2 mm^2
Power (0.18µ)	0.5 mW/MHz	0.5 mW/MHz	0.5 mW/MHz
Power (0.25µ)	1 mW/MHz	1 mW/MHz	1 mW/MHz

*Dhrystone 2.1 MIPS

Mips says the 4Km soft core is available now and has already been licensed to Texas Instruments for use in its ASIC library, and to Lara Technologies, a startup that's developing a voice-over-IP product. For customers who would rather not port the synthesizable model to an IC process themselves, Mips has also licensed the 4Km core to Chartered Semiconductor, which will offer a prehardened core on a 0.25-micron process in 4Q99 and on a 0.18-micron process in 1Q00. Obtaining the prehardened core from Chartered also allows customers to avoid paying an upfront licensing fee by signing a simplified MIPS license with predefined royalties (see MPR 7/12/99, p. 7).

The 4Km is a relatively minor variation on the existing 4Kc and 4Kp cores, but it underlines Mips's renewed push into the embedded-processor market. At Microprocessor Forum this week, Mips is announcing the first 64-bit synthesizable core based on the MIPS64 instruction-set architecture (the 5Kc, code-named Opal). The 4Km and 4Kc cores compete directly with the ARM9E core (see MPR 6/21/99, p. 11) and offer comparable performance, power consumption, and MAC capabilities. —*T.R.H.*