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ARM's Asynchronous Handshake

Handshake Solutions Designs Asynchronous ARM9 Processor Core

By Tom R. Halfhill {11/29/04-02}

Asynchronous logic is one of those promising technologies that seem perpetually just around the corner, like artificial intelligence, reliable speech recognition, and reconfigurable logic. Universities pour forth a steady stream of papers on the subject. Academicians and corporate scientists hobnob at brainy conferences. Investors sink money into startup companies that stall just short of commercial success. Reporters and analysts write thrilling articles about how the technology is about to turn the corner.

From its roots in the 1950s, asynchronous logic has captivated circuit designers who yearn to break the bonds of clock-timed logic and create free-running processors that work at their own pace. It's been done many times, in many different ways, but conventional synchronous technology is too entrenched. In the past, asynchronous processors haven't offered enough advantages over conventional processors to make significant headway in the marketplace. Now, ARM and Handshake Solutions (a line of business within Royal Philips Electronics in the Netherlands) think conditions are changing in favor of asynchronous logic—at least on a small scale that promises some hope of commercial success.

What's changing is the power-consumption curve in deep-submicron fabrication processes. Leakage current is becoming as important as dynamic current, and dynamic current is rising because of the growing complexity of circuits in modern microprocessors. Even with extensive clock gating, large numbers of transistors in synchronous processors remain powered when they aren't doing actual work. Either the transistors are part of circuits that can't easily be shut down in a clocked processor (including the clock-propagation logic itself), or they are holding intermediate results in flip-flop registers. Although some asynchronous-logic projects strive for higher throughput, ARM and Handshake Solutions are trying to reduce power consumption, silicon costs, and electromagnetic interference (EMI). Those goals are vital for deeply embedded processors in such applications as smartcards, control-area networks (CAN), and wireless communications devices.

ARM has had its hands in asynchronous logic for more than a decade, mainly by working with Manchester University in England, a longtime pioneer of the technology. Manchester built the asynchronous MU5 computer in 1969–1974 and in the early 1990s designed three asynchronous ARM-compatible processors: the Amulet 1, Amulet 2, and Amulet 3e. None reached the market, although the Amulet 3e nearly made it into a wireless base station until the customer was acquired by another company and the deal fell through. In general, the Amulet chips had superior power management and emitted significantly less EMI than comparable ARM-based processors, but they required more effort to design. All were based on Ivan Sutherland's micropipelined asynchronous-logic technology. (See *MPR 2/25/02-01*, "Technology 2001: On a Clear Day You Can See Forever.")

Handshake Solutions is taking a different approach. Its asynchronous logic is based on proprietary technology and design tools developed by Philips with commercial exploitation firmly in mind. The biggest challenge of asynchronous logic isn't to make it work—as mentioned before, it's been done many times, in different ways—but to make it fit into existing design flows. To be commercially successful, the

asynchronous logic must not require full-custom circuit design; it must be easy to integrate with synchronous logic blocks on the same chip and with other chips; the special design tools must work with conventional design tools; the asynchronous portions of a design must be as easy to test and verify as the synchronous portions; and the finished design must be compatible with standard fabrication processes at popular foundries. Too many other projects have focused primarily on the circuit-level aspects of asynchronous logic.

The Philips project, originally known as Tangram, was regrouped as Handshake Solutions within the Philips Technology Incubator. As a newly minted ARM licensee, Handshake Solutions has been working closely with ARM to design a fully asynchronous ARM9 processor core that ARM will license commercially in 1Q05. The asynchronous core is compatible with the ARMv5TE instruction-set architecture and is a wholly new member of the ARM9 family, not simply an asynchronous port of an existing ARM9 design. A lead customer (as yet undisclosed) is about to license the core.

Although ARM and Handshake Solutions won't release performance details until later this year, the new core is supposed to consume significantly less power and emit much less EMI than a synchronous ARM9 core. *Microprocessor Report*'s analysis of previous asynchronous designs and other factors indicates the new ARM9 core might use only 30–50% as much power as a synchronous ARM9 with similar performance.

First Commercial Asynchronous 32-Bit CPU

Most previous attempts to design a fully asynchronous microprocessor have limited their ambitions to eight-bit designs. For example, Theseus Logic, founded in 1996, introduced the eight-bit NCL08 in September 2000. This microcontroller core is compatible with the Freescale HCS08 architecture and uses the Theseus proprietary Null Conventional Logic (NCL), a low-power asynchronous-logic technology described in our 2002 article referenced above. However, Theseus is now moving toward becoming a fabless semiconductor company. Next year, Theseus plans to release an asynchronous 8051-compatible microcontroller that integrates flash memory, SRAM, an encryption engine, and an IEEE 802.15.4 "Zigbee" radio on a single chip. This device is intended to be a low-power, low-EMI microcontroller for wireless sensor systems.

Handshake Solutions also has extensive experience with eight-bit asynchronous logic. Its team has produced and sold an asynchronous 80C51-compatible microcontroller since 1995. This chip is slightly larger than a conventional 80C51 (about 6,000 gates vs. 5,600 gates), but it consumes only about 33% as much power while delivering about 50% more throughput.

Figure 1 compares infrared thermal photographs of the active-power "hot spots" in the asynchronous 80C51 and a synchronous 80C51. During the past nine years, millions of these microcontrollers and related ICs have found their way into pagers, analog cordless phones, wireless videogame consoles, smartcards, automotive networks, and passports with radio-frequency identification (RFID) chips storing biometric data. All Philips Semiconductor's MifareProX and SmartMX smartcards use Handshake Solutions' asynchronous chips. Until now, however, Handshake Solutions has not applied its technology to a 32-bit microprocessor architecture—a considerably more difficult undertaking.

The new ARM9 core developed by Handshake Solutions and ARM will be the first fully asynchronous 32-bit processor core to be marketed commercially. The Amulet processors designed at Manchester were fully asynchronous 32-bit designs, but, as we noted, they never reached the market. Another fully asynchronous 32-bit processor was produced at the California Institute of Technology (Caltech) in 1998, but it never became a commercial product, either. That processor was the briefly famous R3000-compatible MiniMIPS. When Hewlett-Packard fabricated some test chips in a 0.6-micron CMOS process, the MiniMIPS reached 250MHz—twice as fast as any other microprocessor manufactured by HP in that process at the time.

Two students who worked on the MiniMIPS project—Andrew Lines and Uri Cummings—later founded Fulcrum Microsystems, a Southern California company specializing in asynchronous logic. Lines and Cummings were soon joined by two other students from the MiniMIPS project. Fulcrum became a MIPS licensee and began designing an asynchronous MIPS32 processor, but the project was shelved two years ago in favor of other products that were less expensive to develop and showed more commercial potential.

Last June, Fulcrum introduced PivotPoint, a SPI-4.2 network-switch chip. PivotPoint is about 85% asynchronous, including the high-speed datapaths, management logic for queues and FIFO buffers, 200KB of SRAM, and a unique on-chip crossbar switch that joins the synchronous

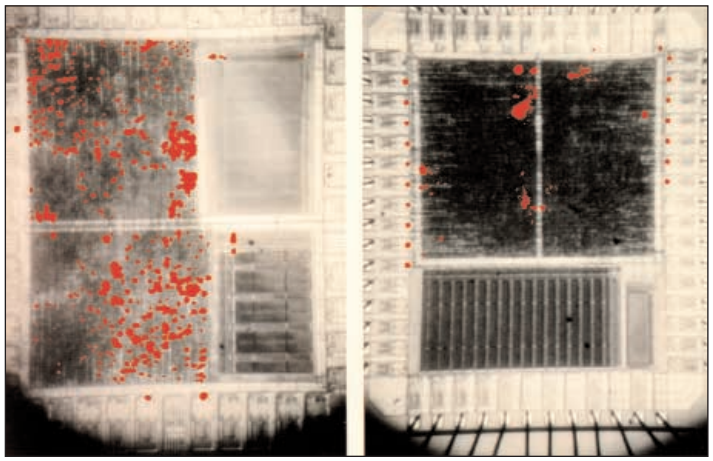

Figure 1. These infrared thermal photographs reveal the hot spots of actively powered circuits in a pair of 80C51-compatible microcontrollers. Handshake Solutions' asynchronous-logic 80C51 is at right; a conventional synchronous 80C51 is at left. Many synchronous circuits are constantly active because of the processor's global clock, whether or not the circuits are performing any tasks. In contrast, the asynchronous logic stays passive until needed.

For More Information About Asynchronous Logic

A wealth of information is available about asynchronous logic, thanks to numerous research projects and commercial ventures dating back to the 1950s. A loosely knit global research and development community keeps the technology very much alive. Last March, for example, hundreds of people attended the Clockless Computing symposium at Washington University in St. Louis, Missouri. Here are some sources for additional research:

Clockless Computing symposium at Washington University in St. Louis:
- *www.cse.seas.wustl.edu/clockless*

Async 2005, the 11th IEEE International Symposium on Asynchronous Circuits and Systems, March 14–16, 2005:
- *http://vlsi.cornell.edu/async2005/*

Asynchronous Logic Home Page (Manchester University):
- *www.cs.man.ac.uk/async*

Manchester University's Amulet project:
- *www.cs.man.ac.uk/apt/projects/processors/amulet/AMULET1_uP.html*

Fulcrum Microsystems:
- *www.fulcrummicro.com*

Theseus Logic:
- *www.theseus.com*

Sun Microsystems' FleetZero project:
- *http://research.sun.com/features/async/*

"Computers without Clocks," by Ivan E. Sutherland and Jo Ebergen, *Scientific American*, August 2002:
- *www.sciam.com/article.cfm?articleID=00013F47-37CF-1D2A-97CA809EC588EEDF&pageNumber=1&catID=2*

"Computer Clocks Wind Down," by Gary H. Anthes, *ComputerWorld*, December 23, 2002:
- *www.computerworld.com/hardwaretopics/hardware/story/0,10801,76931,00.html*

and asynchronous logic blocks. Fulcrum has licensed this crossbar interconnect technology, called Nexus, to PMC-Sierra, which recently introduced the asynchronous crossbar in its new RM11200 at Fall Processor Forum 2004. (See *MPR 10/25/04-01*, "Embedded CPUs Zoom at FPF.")

Making Power-Performance Trade-offs

Fulcrum's asynchronous logic aims for high throughput. In contrast, ARM and Handshake Solutions are aiming for lower dynamic power, low cost, and reduced EMI. The choice of a performance target greatly influences the flavor of asynchronous logic.

All forms of asynchronous logic replace the lockstep regulation of a global clock with some kind of handshaking protocol between logic blocks. Handshaking is necessary because the self-timed circuits won't complete their tasks at regular, predictable intervals. A logic block sends a handshake signal when it's ready to forward its results to the next logic block in the circuit. Likewise, the next logic block returns a signal when it's ready to receive the data. In concept, it's like the handshaking between computer peripherals that can't deliver predictable performance because of unknown interface latencies, such as the ACK and NAK signals between modems on either end of a telephone line. The differences among asynchronous-logic circuits essentially boil down to the protocol format and the number of wires carrying the data signals.

In the new asynchronous ARM9 core, Handshake Solutions uses a four-phase single-rail design. The handshaking protocol uses four-phase control signaling (the equivalent of ACK and NAK requests and responses) over two wires between every logic block. Each bit in the datapath requires one wire (rail), or 32 wires for a 32-bit datapath. Figure 2 illustrates the control signaling between an active logic block that's ready to pass along data to the next logic block, which is currently passive.

Single-rail datapaths are typical of asynchronous designs aiming for low power consumption. In contrast, Fulcrum's high-performance asynchronous technology uses a four-phase dual-rail design coupled with fast domino logic and relatively large transistors. A typical dual-rail datapath requires two wires per bit, although Fulcrum uses a more efficient one-of-*n* encoding scheme. Handshake Solutions' single-rail technology is slower than dual rails, but it reduces the number of data wires between logic blocks. The less complex wiring and lower-performance circuits should reduce the silicon area required for the layout. Theoretically, the smaller layout could cut power consumption by about half compared with the performance-optimized dual-rail approach.

There is some overhead in all asynchronous logic because of the control wires, but Handshake Solutions compensates by substituting latches for many of the flip-flops in synchronous logic circuits. Because the processor's "clock frequency" (actually, the self-timed operating frequency of the asynchronous logic) ebbs and flows with the workload instead of oscillating at a high enough frequency to handle the biggest

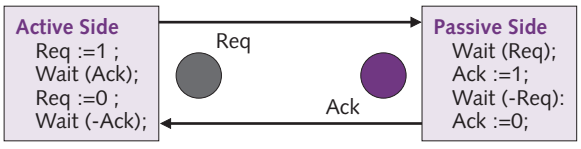

Figure 2. Handshake Solutions' four-phase signaling requires two control wires to carry requests and responses between blocks of asynchronous logic. Data doesn't move from one block to another until both have signaled their readiness. This illustration omits the 32 additional wires required for a single-rail 32-bit datapath between the blocks.

Price & Availability

ARM's new asynchronous ARM9 processor core is scheduled to be available for general licensing in 1Q05. ARM hasn't disclosed licensing terms and prices, but they are expected to be similar to those for other ARM9-family cores. Separately, Handshake Solutions licenses its proprietary tools for customers wanting to design their own asynchronous logic. License fees are variable; a standard, nonfloating seat license for a multiuser customer is €50,000 (about US$64,775). For more information, visit *www.arm.com/news/6936.html* and *www.handshakesolutions.com*.

anticipated workload, the chip overall should require fewer gates, consume less power, and emit less EMI than a similar processor implemented in synchronous logic.

Standard Design Flow Makes the Difference

The power-performance trade-offs of single-rail and dual-rail asynchronous logic are well established. Likewise, the trade-offs of various handshaking protocols are well understood. What sets the ARM–Handshake Solutions collaboration apart from previous projects is the attempt to market a fully asynchronous 32-bit processor that fits seamlessly into existing design flows.

Most customers probably wouldn't license the new ARM core if it isn't easy to integrate with their own synchronous logic and the licensable intellectual property (IP) required to design a modern ASIC or SoC. Ideally, an asynchronous core should work with industry-standard electronic-design automation (EDA) tools, standard cell libraries, everyday test-and-verification techniques, and common fabrication processes. It's this kind of start-to-finish design integration that has tripped up some other asynchronous-logic projects. ARM and Handshake Solutions say they have achieved all these objectives.

```
Top : main proc (a?chan int & b!chan int).
begin x : var int |
   forever do a?x ; b!x+1 od
end
```

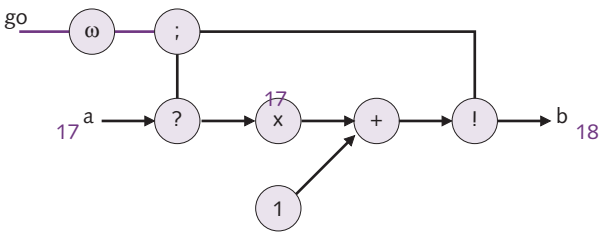

Figure 3. Handshake Solutions' proprietary Haste language allows circuit designers to create asynchronous logic by starting with a high-level behavioral description. Haste is intended to be as easy to use as behavioral Verilog is. Although Handshake Solutions licenses Haste and its other proprietary tools to customers wanting to design their own asynchronous logic, licensees of the new asynchronous ARM9 core need never see these tools—they will receive a physical description of the core already prepared for standard place-and-route tools.

ARM licensees won't have to design asynchronous logic or mess with its details. The new processor is a "firm core," halfway between a synthesizable soft core and the fixed layout of a hard core. Licensees will receive a gate-level physical description of the ARM9 core, ready for place and route. It's compatible with the standard cells of any physical library, any fabrication process, and any foundry. Although the processor core is fully asynchronous, the I/O interfaces are synchronous and function normally. There's still a clock for controlling I/O. Customers can drop the new processor into a chip design and integrate it with any other synchronous logic, just as they would with any ARM core.

Equally important, the asynchronous ARM9 processor is compatible with existing design-for-test methods and verification tools. To the outside world, it appears to be a conventional synchronous core. It works with standard scan chains and test-pattern generators, so customers can achieve the same quality of testing and verification that they can with a conventional processor core. Previous asynchronous processors usually required special tools that don't mate with existing design flows.

Although Handshake Solutions' key innovation is back-end tools that hide the low-level details of asynchronous logic from circuit designers, ARM licensees won't need these tools at all, unless they want to create their own asynchronous logic. Handshake Solutions licenses its proprietary tools separately and also offers design services.

The first link in Handshake Solutions' proprietary tool chain is an abstract circuit-design language called Haste. It bears a resemblance to software languages like C and hardware-design languages like behavioral Verilog, and it has special constructs for expressing parallelism and sharing resources. Haste draws upon a preconfigured library of about 50 asynchronous-logic components, including data registers, arithmetic units (adders, multipliers), bit shifters, multiplexers, and control structures (if-then-else, while-do). Many components support multiple data types in both signed and unsigned varieties. Handshake Solutions' proprietary Haste compiler translates the high-level behavioral design into combinations of these circuit components. Figure 3 shows how a few lines of Haste code produce a simple circuit.

Another proprietary tool, *HT Mapper*, takes the output of the Haste compiler and produces a conventional Verilog netlist by mapping the design onto standard cells. At this point, the asynchronous design is compatible with industry-standard EDA tools from the likes of Cadence, Mentor, Synopsys, and Synplicity. Customers can use conventional tools to optimize the logic, insert scan chains, adjust the timing, and map the design to physical libraries.

Clock Speed Gets Even More Meaningless

Handshake Solutions says its proprietary design tools also ease the integration of analog circuits and RF components on a chip with synchronous and asynchronous digital logic. When combined with the reduced power consumption and EMI of an asynchronous design, these characteristics make the technology particularly suitable for low-power wireless applications, such as RFID chips and communications devices. Of course, we won't know how well these advantages carry over to the new ARM9 core until the first silicon is available for characterization. Handshake Solutions expects its lead customer to receive the first production silicon around 3Q05.

Even when chips are available, evaluating them will require some mental adjustments. Clock frequency, already an imperfect yardstick for comparing processors, becomes even less meaningful with a processor built of clockless logic. Eventually, ARM plans to run EEMBC benchmarks on the new processor core and release certified scores. Doing that will allow direct comparisons with other 32-bit embedded processors in its class—including synchronous ARM9 cores, which should be most illuminating. Until then, ARM will probably give customers a rough estimate of performance by expressing a "typical" clock frequency for a general-purpose workload, much as vendors estimate the typical power consumption of a processor under similarly vague conditions.

Speaking of power consumption, ARM will probably specify a range of dynamic power for the new processor, perhaps with a worst-case estimate of peak power. For now, ARM is reluctant to promise how much power the asynchronous logic will save. *MPR* estimates the asynchronous ARM9 core will use 30–50% less power than a synchronous ARM9 with similar performance. In any event, these necessarily broad guesstimates of power consumption will make it even more imperative for EEMBC to finish its long-running project of defining consistent power-consumption benchmarks.

Potential Payoff Is Huge

Too little is known about ARM's latest fling with asynchronous logic to judge whether it will succeed where previous attempts have fallen short. Although the Amulet project at Manchester never led to a successful commercial product, ARM surely learned something from the experience that justifies its faith in Handshake Solutions' technology. Nevertheless, ARM is climbing out on a limb by promising to soon deliver the first commercial 32-bit microprocessor core implemented in asynchronous logic.

If ARM's gamble is successful, the payoff could be huge. Already, ARM has established itself as the leading vendor of low-power embedded processor cores. Anything that further slices the power consumption of ARM's processors by a significant amount will strengthen the company's leadership position and fend off competition from ARC International, MIPS Technologies, and Tensilica. In addition, significantly reducing EMI would make ARM processors even more compelling for wireless phones, other mobile communications devices, and CANs in automobiles, aircraft, and industrial equipment. A successful asynchronous processor might even make Handshake Solutions an attractive acquisition target for ARM, which has been in an acquisitive mood lately. (See *MPR 9/7/04-01*, "ARM Extends Its Reach.") As things now stand, anybody could license Handshake Solutions' proprietary tools and try duplicating the feat.

Given the false hopes and failed experiments of the past, we hesitate to crawl out on the same limb and declare that ARM and Handshake Solutions have turned the corner on asynchronous logic. But unless the first silicon is a surprising disappointment, it appears the two companies have scored a breakthrough. ◇