



FREESCALE UPGRADES QORIQ

Faster P1- and P2-Series Processors, Plus New PowerQuicc Chips

By Tom R. Halfhill {9/6/10-01}

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Faster packet processing is getting cheaper. Freescale is adding packet-acceleration hardware to the QorIQ P1 and P2 series, matching a feature previously available only in the higher-priced P3, P4, and P5 series. At the same time, Freescale announced a new series of PowerQuicc II Pro chips, reassuring customers that the older PowerQuicc family lives on.

The new QorIQ chips are the single-core P1017, dual-core P1023, and quad-core P2040, which are summarized in Table 1. All have Freescale's Data-Path Acceleration Architecture (DPAA)—a fancy name for the packetacceleration hardware that first appeared in the eight-core P4080, Freescale's largest networking chip. Extending DPAA to the lower-priced chips allows software developers to use the same code, tools, drivers, frameworks, and application programming interfaces (APIs) across the whole QorIQ family.

All three new P-series processors also have Freescale's newest security engine (SEC 4.2), which offloads cryptography processing. The P1 chips use Freescale's Power e500v2 CPU core, but the P2040 has the improved Power e500mc, which includes hardware support for a Type 1 hypervisor—a unique feature among embedded processors. All the newly announced QorIQ chips are scheduled to start sampling in 1Q11; we estimate production availability by 1Q12. Freescale hasn't announced pricing, but we estimate the new P1 and P2 chips will cost less than \$50 and the P2040 will cost about \$100 in volume.

Meanwhile, Freescale isn't ignoring customers who have been using PowerQuicc processors since the 1990s. The new PowerQuicc II Pro MPC830x series updates the older family with DDR2 memory controllers, PCI Express (PCIe), and Secure Digital High Capacity (SDHC) memory-card interfaces (useful for firmware). Coming two years after Freescale's introduction of the QorIQ family, a new PowerQuicc series is a surprise. But Freescale wants to please loyal customers, who may be more disposed to look favorably on QorIQ when it's eventually time to upgrade.

Four Cores for Fewer Bucks

The most interesting new QorIQ processor is the quadcore P2040, which appears to be a derivative of the quadcore P3041. So far, the P3041 is the sole member of the P3 series, which Freescale announced in June at the same time as the new P5 series. (See *MPR* 7/5/10-01, "Freescale P5 Raises QorIQ's I.Q.")

	QorlQ P1017	QorlQ P1023	QorlQ P2040	
СРИ Туре	Power e500v2	Power e500v2	Power e500mc	
CPUs per Chip	1 CPU	2 CPUs	4 CPUs	
CPU Freq (max)	800	1.2GHz		
L2 Cache	25	1MB		
Memory Controller	DDR2 32 up to 6	DDR3 / 3L, 32 / 64 bits, up to 1.2GHz ECC		
Ethernet Cntlrs	2x	5x GbE		
PCI Express	3x PC	3x PCIe 2.0		
Other I/O	USB, SPI		SATA, sRIO, USB, SPI	
On-Chip Network	PowerC	CoreNet fabric		
IP Forwarding	Up to	Up to 5Gb/s		
Power (max)	2.5–3.0W	3.0–3.5W	~10W	
Availability	Samples 1Q11 (est), production 1Q12*			

Table 1. New processors in Freescale's QorlQ family. The most interesting new member is the quad-core P2040, which is a lower-priced version of the quad-core P3041 and is probably derived from the same die. (Source: Freescale, except *The Linley Group estimate)

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As Figure 1 shows, the P2040 is essentially a slower, economized version of the P3041. In addition to eliminating one PCIe port, the 10G Ethernet interface, and the 512KB L2 cache, it sheds 512 of the P3041's 1,295 pins, breaking pin compatibility with the P3041 but reducing the packaging costs. Also, the P2040's maximum target clock speed is 1.2GHz—20% slower than the P3041's top speed. Freescale estimates that a 1.2GHz P2040 will consume about 10W (maximum)—33% less than a 1.5GHz P3041. We estimate the price will drop by approximately the same degree to about \$100.

As a P3041 derivative, the P2040 is the first member of the P2 series to have the new CoreNet Coherency Fabric instead of the simpler bus architecture inherited from the legacy PowerQuicc line. CoreNet scales much better than a multidrop bus for multicore designs having more than two CPUs. (See *MPR* 7/7/08-01, "Freescale's Multicore Makeover.")

Likewise, the P2040 is the first of the P2 series to use Power e500mc cores instead of the older Power e500v2. Until now, only P3 and P4 chips used the Power e500mc. Among other features, the Power e500mc has extensions that improve the performance of multiple operating systems (or multiple instances of the same operating system) running concurrently on a hypervisor. The hypervisor can share the P2040's Ethernet and PCIe ports among multiple operating systems by virtualizing control registers and by



Figure 1. Freescale QorlQ P2040 block diagram. This close relative of the QorlQ P3041 eliminates some features and reduces the maximum target clock speed but cuts both cost and power. It will be Freescale's most economical quad-core networking processor.

intercepting I/O requests and exceptions and routing them to the appropriate CPU. (See the sidebar, "The New, Improved Power e500mc Processor Core," in *MPR* 7/7/08-01, "Freescale's Multicore Makeover.")

By retaining the P3041's DPAA packet-acceleration hardware and SEC 4.2 security engine as well, the P2040 will make life a little easier for system designers, at least on the software side. Software compatibility with the P3041 means that developers can design different models of routers, gateways, security appliances, and other systems for different price/performance points without rewriting all their software. (Freescale says that SEC 4.2 can accelerate IPSec throughput by 45% to 75% compared with the older SEC 3.x engines.)

On the hardware side, system designers making multiple products must do a little more work, because the P2040 isn't pin compatible with the P3041 or any other QorIQ chips. But Freescale says future QorIQ processors will be pin compatible with the P2040. Those future processors could be additional P2-series chips or the T-series QorIQ processors that Freescale has yet to announce.

The P2040 is designed primarily for fixed routers, 4G-cellular base stations (channel cards), and enterprise security applications. Our estimate of 1Q12 production is based on Freescale's fairly consistent history of shipping new products in volume about one year after the first samples appear.

Lower Power Than Competitors

Microprocessor Report analyzed the P3041 in our previously cited July article, noting that the chip is an economymodel alternative to the very similar QorIQ P4040. By extension, the P2040 isn't radically different from the P4040, either, except it consumes less than half the power. (As a first-generation QorIQ design that was cut down from the eight-core P4080, the P4040's days seem numbered, unless a developer needs twice as much memory bandwidth as the P3041 and P2040 provide.)

We reviewed the P3041 favorably and saw it as a logical replacement for several older chips: the PowerQuicc III MPC8548E, MPC8536E, MPC8544E, and MPC8572E and the MPC8641D. We also compared the P3041 with two competing chips: Cavium's Octeon II CN6330 and NetLogic's XLS616. Since then, NetLogic has unveiled its new XLP family, which will be more competitive with Freescale's newest QorIQ chips. (See MPR 7/26/10-01, "NetLogic Broadens XLP Family.") Table 2 com-

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pares Cavium's CN6330 and NetLogic's XLP208 with the QorIQ P2040.

The P2040 is clearly the lowest-power choice, assuming the vendors' power estimates are close to accurate. It's not hard to see why: the P2040 is simply a lesspowerful networking processor. It's a 32-bit implementation of the Power Architecture (Cavium and NetLogic are MIPS64 compatible), it has the lowest maximum clock speed (partly because of its shorter instruction pipeline), it has the smallest L1 caches and no L2 cache, it has the lowest pin count, and it's the only processor in this group without an optional 10G Ethernet interface.

NetLogic's XLP208 would seem to be handicapped in this comparison by having only two CPU cores, instead of four cores like the other chips. But the XLP208's target clock speed is 67% faster than the P2040's, and NetLogic's EC4400 CPUs can issue twice as many instructions per

clock cycle. Moreover, each EC4400 CPU can manage four threads—it's the only multithreaded design in this group. Particularly in applications that mix control-plane and data-plane processing, the XLP208 will beat the P2040 and could even give the P3041 a run for its money.

With more cache, more memory bandwidth, and more I/O interfaces than the other processors, the XLP208 is clearly the most capable processor in this group. Although it burns about 50% more power than the P2040, its dynamic voltage/frequency scaling should reduce typical power nearer to the level of the P2040. Still, the P2040 remains the best low-power option for system designs needing less I/O. It will almost certainly cost less, too—about 43% less, in our estimation.

Keep in mind that none of these processors is sampling yet, so production schedules and specifications could change before these chips reach customers. NetLogic's schedule is more aggressive than Freescale's and Cavium's, anticipating progress from sampling to production in only nine months. That ramp is optimistic when moving to a new process generation with a new and untested CPU core. A little slippage could push the XLP208 into the same time frame as the P2040 and P3041.

P1 Cuts Power Below 3.0W

The new P1-series processors aren't as impressive as the P2040, but they bring

Freescale's packet-acceleration hardware and SEC 4.2 security engine to the least-expensive (less than \$50) series in the QorIQ family. The P1017 and P1023 are designed for 802.11n wireless access points, small-business gateways, and low-end fixed routers. With three PCIe controllers, they can connect to three different radios in wireless routers. DPAA packet acceleration offloads some routing chores from the CPUs, and the security engine offloads cryptography processing. These chips lack a regular-expression engine, however.

The P1017 has only one CPU and appears to be the lowest-power member of the P1 series. Freescale estimates the P1017 will consume only 2.5W to 3.0W (maximum). The company says the dual-core P1023 will consume 3.0W to 3.5W, so the additional CPU levies only a half-watt penalty. All P1 chips fit within a 5.0W envelope—these are the chips to use in small systems with passive cooling.

	Freescale	Freescale	Cavium	NetLogic
	QorlQ P2040	QorlQ P3041	Octeon II CN6330	
CPU Type	Power e500mc	Power e500mc	cnMIPS64-R2	EC4400
Arch. Width	32 bits	32 bits	64 bits	64 bits
Pipeline	7 stages	7 stages	9 stages	12 stages
Issue Rate	2 per cycle	2 per cycle	2 per cycle	4 per cycle
CPUs per Chip	4 CPUs	4 CPUs	4 CPUs	2 CPUs
Multithreading	—	—	—	4 threads per CPU
CPU Freq (max)	1.2GHz	1.5GHz	1.5GHz	2.0GHz
L1 Cache	32KB / 32KB	32KB / 32KB	37KB / 32KB	64KB / 32KB
(I / D)	per CPU	per CPU	per CPU	per CPU
L2 Cache	—	128KB per CPU	2MB shared ECC	512KB per CPU
L3 Cache	1MB shared,	1MB shared,		2MB shared,
L3 Cache	ECC	ECC	_	ECC
	DDR3 / 3L,	DDR3 / 3L,	DDR3,	DDR3,
Memory	1x 32 / 64 bits,	1x 32 / 64 bits,	1x 64 bits,	1x 64 bits,
Controller	up to 1.2GHz,	up to 1.3GHz,	up to 1.6GHz,	1.6GHz,
	ECC	ECC	ECC	ECC
PCI Express	3x PCIe	4x PCIe	2x PCIe	4x PCle
Ethernet	5x GbE	5x GbE	4x GbE	8x GbE
Controllers	JX GDL	1x 10GbE	or 1x 10GbE	or 1x 10GbE
Serdes	10 lanes	18 lanes	12 lanes	20 lanes
Serial RapidIO	2x sRIO	2x sRIO	1x sRIO	4x sRIO
USB 2.0	2 with PHYs	2 with PHYs	2 with PHYs	4 with PHYs
Serial ATA	2x 3Gb/s	2x 3Gb/s	—	4x 3Gb/s
RAID Engine	—	—	RAID5 / RAID6	RAID5 / RAID6
Crypto Accel?	Yes	Yes	Yes	Yes
Reg-Ex Engine?	Yes	Yes	Yes	Yes
IC Process	45nm SOI	45nm SOI	65nm G	40nm G
Voltage (CPU)	1.0V	1.0V	Not disclosed	0.7–1.1V
Power (max)	~10W	15W	17W	15W
	FC-PBGA,	FC-PBGA,	FCBGA,	BGA.
Package	783 pins,	1,295 pins,	900 pins,	~1,000 pins
	23mm	37.5mm	31mm	
Sampling	1Q11 (est)	4Q10 (est)	2Q10	4Q10 (est)
Production	1Q12*	2H11 (est)	2Q11 (est)	3Q11 (est)
List Price	\$100*	\$150*	\$150*	\$175*

Table 2. Comparing Freescale's P2040 with Cavium and NetLogic competitors. The P2040 is the lowest-power processor in this group, but it sacrifices some features and performance to get there. Although we lack firm pricing from vendors, the P2040 will probably be the smallest and least-expensive chip in this group. (Source: vendors, except *The Linley Group estimate)

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Otherwise, the P1023 is identical to the P1017, including having the same 19mm 457-pin package (a thermally enhanced plastic ball-grid array, or TEPBGA). Both are fabricated in 45nm SOI, and clock frequencies will range from 400MHz to 800MHz. Note that both processors have the older PowerQuicc bus instead of the CoreNet fabric, and both have the older Power e500v2 CPU instead of the Power e500mc. Neither legacy is a handicap for single- or dual-core processors intended for small low-power systems.

PowerQuicc Soldiers On

Four new PowerQuicc II Pro chips form the MPC830x series: the MPC8306, MPC8306S, MPC8308, and the MPC8309. Although Freescale introduced the QorIQ family in 2008 to eventually supersede the PowerQuicc line, many existing customers still use PowerQuicc chips and want an upgrade that doesn't require a leap to QorIQ at this time. Freescale's longevity program promises availability for 10–15 years after the product launch, a lifespan that's unthinkable in other microprocessor realms.

Actually, one of the new chips (the MPC8308) was quietly introduced last year, and Freescale is already ramping production. It's the only MPC830x processor without Freescale's Quicc engine, which offloads some networking

	MPC8306	MPC8306S	MPC8308	MPC8309
CPU Freq	133–266MHz	133–266MHz	266–400MHz	266–400MHz
L1 Cache (I/D)	16KB / 16KB	16KB / 16KB	16KB / 16KB	16KB / 16KB
Memory Controller	DDR2, 16 bits, up to 266MHz	DDR2, 16 bits, up to 266MHz	DDR2, 16 / 32 bits, up to 333MHz, ECC	DDR2, 16 / 32 bits, up to 266MHz, ECC
PCI / PCIe	_	_	1x PCIe	1x PCI 2.3
Ethernet	Up to 3x	Up to 3x	2x	Up to 3x
Controllers	Fast Ethernet	Fast Ethernet	10 / 100 / 1000	Fast Ethernet
USB 2.0	1x USB 2.0	1x USB 2.0	1x USB 2.0	1x USB 2.0
HDLC / TDM	2x HDLC / TDM	2x HDLC / TDM	—	2x HDLC / TDM
CAN	4x CAN	_	_	4x CAN
Misc I/O	2x DUART, I ² C, SPI, GTM, GPIO, SDHC	2x DUART, I ² C, SPI, GTM, GPIO	1x DUART, I ² C, SPI, GTM, GPIO, SDHC	2x DUART, I ² C, SPI, GTM, GPIO, SDHC
IEEE1588?	Yes	No	Yes	Yes
Quicc Engine?	Yes	Yes	No	Yes
IC Process	90nm	90nm	90nm	90nm
Power (typ)	1.15W @ 266MHz	1.15W @ 266MHz	1.23W @ 333MHz	1.56W @ 333MHz
	MAPBGA,	MAPBGA,	MAPBGA,	MAPBGA,
Package	369 pins,	369 pins,	473 pins,	489 pins,
	19mm	19mm	19mm	19mm
Sampling	3Q10	3Q10	4Q09	3Q10
Production	4Q10 (est)	4Q10 (est)	In production	1Q11 (est)
Resale List Price	\$7.36	< \$10	\$9.94	< \$10

Table 3. Key parameters for the new PowerQuicc MPC830x processors. All use the 32-bit Power e300c3 core, which has a four-stage pipeline and issues two instructions per cycle. Note that the Power e300c3 core has only half as much L1 cache as some previous Power e300 cores; otherwise, it's virtually identical to the core originally derived from the PowerPC 603e. Despite fabrication in an older 90nm process, all these chips typically use less than 1.6W. (Source: Freescale)

chores from the CPU. The Quicc engine is useful mainly for older and slower network interfaces, so it's unnecessary in the MPC8308. As Table 3 shows, the MPC8308 is the only member of this series with Gigabit Ethernet (GbE) and PCIe interfaces. This processor is designed primarily for entry-level networking applications (wireless access points and femtocell base stations), consumer printers, industrial controls, and factory equipment.

The MPC8306 is designed for similar applications but has the Quicc engine, slower network connections, no PCIe, and no error correction codes (ECC) for main memory. It adds four control-area network (CAN) interfaces, however, so it's suitable for some lower-cost industrial applications and test equipment. A close cousin of this chip, the MPC8306S, eliminates the SDHC interface, drops the IEEE1588 time-stamper for Ethernet packet processing, and kicks the CAN. Freescale is pitching the MPC8306S for low-end base-station line cards and branchaccess gateways.

The MPC8309 is almost identical to the MPC8306 (including a Quicc engine), but it adds a 32-bit DDR2 memory controller with ECC and a PCI 2.3 interface (not PCIe) for networking and industrial equipment that still uses the older flavor of PCI. It's a thoughtful bone to throw to customers who are stuck with legacy systems. SDHC is

another longevity feature. System designers can provide an SD interface to load firmware from a memory card instead of relying on discrete flash memory that quickly becomes obsolete.

All these MPC830x processors update the main memory controller from DDR to DDR2. Given their expected longevity of 10 years or more, DDR3 would seem a wiser choice, but Freescale says DDR3 would have bloated the die, added more pins, and made the sub-\$10 resale price target too difficult to reach with 90nm fabrication. Also, the minimum amount of memory required for a DDR3 interface is probably larger than would be needed by the likely customers for these PowerQuicc chips. DDR3 requires 1Gb to 4Gb of RAM, whereas DDR2 works with 256Mb to 4Gb. The higher cost of more memory offsets DDR3's lower cost per megabit-at least until DDR2 memory becomes scarce.

Trickle-Down Features

Freescale's continuing commitment to PowerQuicc users should reassure QorIQ users as well—nobody likes to design systems for which critical parts The biggest news in Freescale's announcements is the QorIQ P2040, which blurs the formerly bright boundary between the QorIQ P2 and P3 series. For the first time, a lower-cost P2 chip has four CPUs, the improved Power e500mc core, and the faster CoreNet fabric, all within a 10W envelope. Despite its P2 numbering, the P2040 is almost certainly derived from the recently announced P3041, bringing similar features to a lower price point and reducing power, albeit with a little less performance and less I/O. The P2040 will improve Freescale's competitive-ness in enterprise and high-end cellular applications.

Similarly, the new P1-series processors gain features previously found only in higher-priced (and higher-power) QorIQ chips—in particular, packet acceleration and security offloading. These chips are well suited to small-business equipment, such as WLAN access points, yet they consume no more than 2.5W to 3.5W. The dual-core P1023 looks especially impressive at these power levels.

Some of the newest QorIQ chips—including the P1017, P1023, P2040, and P3041—appear to be a 1.5 generation of QorIQ products. Although they are fabricated in

Price & Availability

Freescale's QorIQ P2040 is scheduled to begin sampling in 1Q11. Freescale hasn't announced pricing; The Linley Group estimates less than \$100. The QorIQ P1017 and P1023 are scheduled to begin sampling in 1Q11. Freescale hasn't announced pricing; we estimate \$20 to \$50. For more information, visit www.freescale.com/qoriq.

The PowerQuicc II Pro MPC8308 is in production now. The MPC8306 and MPC8306S are scheduled to begin production next quarter, followed in 1Q11 by the MPC8309. Volume resale prices range from \$7.36 to \$9.94. For more information, point your browser to *www.freescale.com/powerquicc.*

the same 45nm process as first-generation QorIQ chips, they adopt features that Freescale has validated in the initial products, spreading those features throughout the family. Clearly, Freescale is building on its experience with QorIQ to make refinements and improvements.

Next on Freescale's roadmap are second-generation QorIQ T-series processors, which will be manufactured in smaller, faster process technologies. But Freescale isn't waiting for the next generation to roll out new features. Some features will be available sooner in these 1.5generation chips and will followed by T-series performance improvements in the future. ◆

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